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| <b>INFORMATION<br/>DISCLOSURE<br/>CITATION</b><br>PTO-1449                    |   | Customer Number:<br>26615 |         | ATTORNEY'S DKT No.<br>H1174          |          | APPLICATION No.<br>Unassigned |  |
|   |   |                           |         | APPLICANT(S)<br>Chih-Yuh Yang et al. |          |                               |  |
|   |   |                           |         | FILING DATE<br>August 4, 2003        |          | GROUP<br>Unassigned           |  |
| <b>U.S. PATENT DOCUMENTS</b>  |   |                           |         |                                      |          |                               |  |
| EXAMINER'S<br>INITIALS  | PATENT NO.  | DATE                      | NAME    | CLASS                                | SUBCLASS | FILING<br>DATE                |  |
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| <b>FOREIGN PATENT DOCUMENTS</b>   |   |                           |         |                                      |          |                               |  |
| EXAMINER'S<br>INITIALS  | PATENT NO.  | DATE                      | COUNTRY | CLASS                                | SUBCLASS | Translation<br>Yes No         |  |
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|   |   |                           |         |                                      |          |                               |  |
| <b>OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, Etc.)</b> |   |                           |         |                                      |          |                               |  |
| FD  | Digh Hisamoto et al., "FinFET-A Self-Aligned Double-Gate MOSFET Scalable to 20 nm," IEEE Transactions on Electron Devices, Vol. 47, No. 12, December 2000, pages 2320-2325.                                       |                           |         |                                      |          |                               |  |
|   | Yang-Kyu Choi et al., "Sub-20nm CMOS FinFET Technologies," 2001 IEEE, IEDM, pages 421-424.  |                           |         |                                      |          |                               |  |
|   | Xuejue Huang et al., "Sub-50 nm P-Channel FinFET," IEEE Transactions on Electron Devices, Vol. 48, No. 5, May 2001, pages 880-886.  |                           |         |                                      |          |                               |  |
|   | Xuejue Huang et al., "Sub 50-nm FinFET: PMOS," 1999 IEEE, IEDM, pages 67-70.  |                           |         |                                      |          |                               |  |
|   | Yang-Kyu Choi et al., "Nanoscale CMOS Spacer FinFET for the Terabit Era," IEEE Electron Device Letters, Vol. 23, No. 1, January 2002, pages 25-27.  |                           |         |                                      |          |                               |  |
|   | Co-pending U.S. Application Serial Number 10/348,758 filed January 23, 2003 entitled, "GERMANIUM MOSFET DEVICES AND METHODS FOR MAKING SAME," Judy Xilin An et al., 22 page specification, 29 sheets of drawings. |                           |         |                                      |          |                               |  |
| EXAMINER<br><i>[Signature]</i>  |   |                           |         | DATE CONSIDERED<br>7/28/04           |          |                               |  |

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